REMARKS

The Office Action dated December 8, 2003, has been received and carefully noted. The above amendment to claim 1, and the following remarks, are submitted as a full and complete response thereto. Applicants respectfully note that no new matter has been entered through the above amendment. Claims 1-23 are pending in the above-cited application and are respectfully submitted for consideration.

Claims 1-10 and 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Simmons et al.* (U.S. Patent No. 6,167,054). Applicants note that while the rejection purports to be made under §102(b), *Simmons et al.* is not prior art with respect to the present application. Claims 1-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Simmons et al.* in view of *Lau et al.* (U.S. Patent No. 5,893,162). The above rejections are respectfully traversed according to the remarks that follow.

The present invention is directed to, according to claim 1, a method of flow control management of data packets is disclosed. The method includes the steps of determining each time data is being written to memory in order to calculate a memory used amount, determining each time data is being freed from memory in order to calculate a memory freed amount, calculating how much total memory is being used using the memory freed amount and the memory used amount and comparing the total memory being used to a first predetermined threshold, wherein when the first predetermined threshold is reached a first threshold command is issued indicating that the first predetermined threshold has been reached and wherein the memory is implemented

as a linked list, with pointers pointing to next memory locations in the linked list and the determining steps are performed when at least one of the pointers is moved.

The present invention is also directed to, according to claim 11, a method of flow control management of data packets is disclosed. The method includes the steps of determining a memory address to which a start pointer is pointing, wherein the start pointer points to a next memory location in a linked list to be read from memory, determining a memory address to which an end of list pointer is pointing, wherein the end of list pointer points to a last memory location in the linked list, calculating from the start pointer and the end of list pointer a number of memory addresses which are being used by the linked list to determine a total amount of memory being used and comparing the total amount of memory being used to a first predetermined threshold, wherein when the first predetermined threshold is reached a first threshold command is issued indicating that the first predetermined threshold has been reached.

The present invention is directed to, according to claim 15, a switch. The switch includes a bus, a memory interface connected to the bus and to a memory, a receive port connected to the bus, the receive port receiving data packets for transmission to the memory through the bus and the memory interface, a transmit port connected to the bus, the transmit port transmitting data packets from the memory through the transmit port out of the switch and a flow control manager connected to the bus. The flow control manager includes a bus monitor that determines when the data packets are being transmitted to the memory and when the data packets are being transmitted from the

memory to the transmit port, a counter that is incremented each time data packets are transmitted to the memory and decremented each time data packets are transmitted from the memory to the transmit port, wherein the counter indicates a memory being used value and a first comparator that compares the counter to a first predetermined threshold, wherein when the counter meets the first predetermined threshold a first threshold command is transmitted across the bus. The memory is implemented as a linked list, with pointers pointing to next memory locations in the linked list.

The present invention is directed to, according to claim 20, a switch. The switch includes a bus, a memory interface connected to the bus and to a memory, a receive port connected to the bus, the receive port receiving data packets for transmission to the memory through the bus and the memory interface, a transmit port connected to the bus, the transmit port transmitting data packets from the memory through the transmit port out of the switch and a flow control manager connected to the bus. The flow control manager includes a start pointer determiner that determines a memory address to which a start pointer is pointing to, wherein the start pointer points to the next memory location in a linked list to be read from memory, a end of list pointer determiner that determines a memory address to which an end of list pointer is pointing, wherein the end of list pointer points to the last memory location in the linked list, a memory used calculator that determines how many memory addresses are being used by the link list to determine a total amount of memory being used and a first comparator that compares the total amount of memory being used to a first predetermined threshold, wherein when the total amount

of memory being used meets the first predetermined threshold a first threshold command is transmitted across the bus.

Simmons et al. is directed to a network having a shared memory architecture for storing data frames has a set of programmable thresholds that specify when flow control should be initiated on full-duplex network ports. Flow control is initiated based on the number of available frame pointers by transmitting a PAUSE frame having a selected PAUSE interval to a transmitting network station. Specifically, a full-duplex port will output a PAUSE frame having a short, medium, or long programmed pause interval if the free buffer pool of available frame pointers falls below a high, medium, or low programmable threshold, respectively. The switch generates variable-length PAUSE control frames to minimize wasting network bandwidth. It is also noted that *Simmons et al.* discloses memory implemented as a linked list.

In the rejection of claims 1-10 and 15-19, Applicants first note that the rejection is improper on its face because it purports to be made under 35 U.S.C. §102(b), when *Simmons et al.* can only be considered as a prior art reference under §102(e). Additionally, the rejection also appears to indicate that limitations added previously to claims 1 and 15 are given no patentable weight or "are not limiting." Applicants respectfully traverse such a position, because the later added portions to claims 1 and 15 are clearly limiting. In claim 1, the determining steps are recited as being performed when the pointers of the linked list memory are moved, which clearly limits a steps of the method. In claim 15, the implementation of the memory as a linked list is a limitation

that would distinguish that claims from switches whose memories are not implemented as a linked list. Reconsideration of the apparent position taken in the rejection of claims 1-10 and 15-19 is respectfully requested.

Claim 1 recites, in part, that "*the* memory is implemented as a linked list, with pointers pointing to next memory locations in the linked list and the determining steps are performed when at least one of the pointers is moved," and claim 15 recites, in part, that "*the* memory is implemented as a linked list, with pointers pointing to next memory locations in the linked list." While the rejection alleges that the overflow area of *Simmons et al.* is implemented with a linked list, the memory to which determining and calculating of memory levels with respect to watermarks is performed is not a linked list memory. As such, *Simmons et al.* cannot anticipate claims 1 and 15 since it fails to teach the adjustment of buffers and control of flow of a linked list memory. *Simmons et al.* also fails to suggest the present invention as discussed below.

Claims 1-23 were rejected over *Simmons et al.* and *Lau et al.* Applicants first note that the rejection is improper because it fails to disclose what elements of the claims are not disclosed by *Simmons et al.* and taught or suggested by *Lau et al.* Such statements are required in order that a *prima facie* case of obviousness be properly presented. See M.P.E.P 706.02(j). It appears that *Lau et al.* is cited in the rejection for its alleged teaching of head and tail pointers, but the use of head and tail pointers are not disclosed to provide the benefits cited in *Lau et al.* The benefits of *Lau et al.*, which are cited as motivation to combine *Simmons et al.* and *Lau et al.*, are disclosed in *Lau et al.* to accrue

from its superior formulation of a linked list and not the use of head and tail pointers. Thus, the benefits ascribed to *Lau et al.* would not provide motivation to combine the references. As such, Applicants respectfully assert that the rejection of claims 1-23 is improper at least for its failure to cite proper motivation for the combination of the references.

Additionally, the rejection provides no motivation for one of ordinary skill in the art to utilize the linked list formulation of *Lau et al.* in the memory management system of *Simmons et al.* The benefits detailed in *Lau et al.* are compared with prior linked list systems and not non-linked list systems recited in *Simmons et al.* for which adjustments to the buffers are performed. As detailed in the rejection, *Simmons et al.* discloses the use of linked list memories for its overflow queue area and arguably could have implemented its main buffer memories as linked lists if such benefits had been appreciated. In view of what is acknowledged in *Simmons et al.* to have utility in the overflow queue area but explicitly not implemented in memory used as buffers and for flow control, *Lau et al.* does not overcome this negative teaching. As such, Applicants respectfully assert that the rejection is improper for failing to teach or suggest all of the elements of the claims.

Additionally, Applicants respectfully assert that the rejection is guided merely by impermissible hindsight reasoning. "To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner show a motivation to combine the references that create the case of obviousness. In other words,

the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." In re Rouffet, 47 USPQ2d 1453 at 1458(CAFC 1998).

Thus, Applicants respectfully assert that any rejection of claims 1, 11, 15 and 20 over *Simmons et al.* and *Lau et al.* would be improper for failing to teach or suggest all of the elements of those claims. On the basis of the above, independent claims 1, 11, 15 and 20 are respectfully asserted to be patentable, and as a consequence the dependent claims 2-10, 12-14, 16-19 and 21-23 are patentable as well. It is therefore respectfully requested that claims 1-23 be allowed and this application be allowed to pass to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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